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EXAMINER	
LEE, CHUN KUAN	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/601,575	EVANS ET AL.	
	Examiner	Art Unit	
	Chun-Kuan (Mike) Lee	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 September 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22,24,25,27-39,41,42,44 and 45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22,24,25,27-39,41,42,44 and 45* is/are rejected.

7)☒ Claim(s) *1-22,24,25,27-39,41,42,44 and 45* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 September 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

RESPONSE TO ARGUMENTS

1. Applicant's arguments with respect to claims 1-22, 24-25, 27-39, 41-42 and 44-45 have been considered but are moot in view of the new ground(s) of rejection. Objection to the Drawing is withdrawn. Currently, claims 23, 26, 40 and 43 are canceled and claims 1-22, 24-25, 27-39, 41-42 and 44-45 are pending for examination.

I. INFORMATION CONCERNING OATH/DECLARATION

Oath/Declaration

2. The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in **37 C.F.R. 1.63.**

II. INFORMATION CONCERNING DRAWINGS

Drawings

3. The applicant's drawings submitted are acceptable for examination purposes.

III. OBJECTIONS TO THE ABSTRACT AND SPECIFICATION

4. The disclosure is objected to because of the multiple instances of misspelling, wherein "synchronising" should be replace with -synchronizing-.

Appropriate correction is required.

5. The abstract of the disclosure is objected to because of the multiple instances of misspelling, wherein "synchronising" should be replace with -synchronizing-. Correction is required. See MPEP § 608.01(b).

IV. OBJECTIONS TO THE CLAIMS

6. Claims 1-22, 24-25, 27-39, 41-42 and 44-45 are objected to because of the multiple instances of misspelling, wherein "synchronising" should be replace with -synchronizing-.

Appropriate correction is required.

V. REJECTIONS BASED ON 35 U.S.C. 112

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 24 and 41 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. It appears unclear as to the dependency of claims 24 and 41, because claims 24 and 41 are dependent on the canceled claims 23 and 40. Currently, the examiner will assume that the claims 24 and 41 are dependent on claims 1 and 29 respectively for examination.

VI. REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1-22, 24-25, 27-39, 41-42 and 44-45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gearty (US Patent 6,477,638) in view of Martin et al. (US Patent 6,381,692).

9. As per claim 1, Gearty teaches a data processing apparatus, comprising:

a main processor (e.g. CPU) configured le to execute a sequence of instructions (col. 6, ll. 29-30: a sequence of instruction sent to CPU), the main processor comprising a first pipeline having a first plurality of pipeline stages (Fig. 3 and col. 6, ll. 14-28: pipeline with many stages is taught);

a coprocessor (e.g. FPU) configured to execute coprocessor instructions in said sequence of instructions (Fig. 2 and col. 5, ll. 44-48), the coprocessor comprising a second pipeline having a second plurality of pipeline stages (Fig. 3 and col. 6, ll. 14-28: pipeline with many stages is taught), and each coprocessor instruction being arranged to be routed through both the first pipeline and the second pipeline (Fig. 3 and col. 6, ll. 29-30: a sequence of instruction is send to both CPU and the FPU); and

at least one synchronizing queue coupling a predetermined pipeline stage in one of the pipelines with a partner pipeline stage in the other of the pipelines (Fig. 6 and col.

11, ll. 19-30: connection between decoding stages), the predetermined pipeline stage being configured to cause a token (e.g. go-token) to be placed in an entry of the synchronizing queue when processing a coprocessor instruction and the partner pipeline stage being configured to process that coprocessor instruction upon receipt of the token from the synchronizing queue, thereby synchronizing the first and second pipelines between the predetermined pipeline stage and the partner pipeline stage (col. 11, ll. 1-18: the "go-token" is taught which is use to synchronize the pipelines).

Gearty does not teach the data processing apparatus, comprising:

a first-in-first-out (FIFO) buffer having a predetermined plurality of entries;

a tag which uniquely identifies the coprocessor instruction to which the token is related; and

synchronizing without passing signals without fix timing between the pipelines.

Martin teaches a system and method comprising:

a first-in-first-out (FIFO) buffer having a predetermined plurality of entries (Fig. 1, ref. 160a, 160b) (col. 9, ll. 14-29);

a tag which uniquely identifies the coprocessor instruction to which the token is related (col. 6, ll. 11-23); and

synchronizing without passing signals with fix timing between the pipelines (col. 1, ll. 41-66), wherein the synchronization is enabled by the asynchronous processor and the inclusion of the FIFO.

It would have been obvious for one of ordinary skill in this art, at the time of invention was made to include Martin's asynchronous processor's FIFO and tag into

Gearty's data processing apparatus for the benefit of implementing asynchronous processor having simpler architecture and faster processing speed (Martin, col. 1, ll. 49-51) to obtain the invention as specified in claim 1.

10. As per claim 2, Gearty and Martin teach all the limitations of claim 1 as discussed above, where Gearty further teaches the data processing apparatus comprising a plurality of said synchronizing queues, each said synchronizing queue coupling a predetermined pipeline stage in one of the pipelines with a partner pipeline stage in the other of the pipelines (Gearty, Fig. 4 and col. 9, ll. 31-48: the stages are connected for synchronization purposes).

11. As per claim 3, Gearty and Martin teach all the limitations of claim 1 as discussed above, where Gearty further teaches the data processing apparatus comprising wherein one of the at least one synchronizing queues is an instruction queue (Gearty, col. 11, ll. 62-67: instruction have to be synchronized), the predetermined pipeline stage is in the first pipeline and is arranged to cause a token identifying a coprocessor instruction to be placed in the instruction queue (Gearty, col. 11, ll. 1-18: a "go-token" is taught which is used to synchronizing the pipelines), and the partner pipeline stage is in the second pipeline and is configured upon receipt of the token to begin processing the coprocessor instruction identified by the token (Gearty, col. 13, ll. 14-35: the coprocessor starts when the go-token instructs it to).

12. As per claim 4, Gearty and Martin teach all the limitations of claim 3 as discussed above, where Gearty further teaches the data processing apparatus comprising wherein the predetermined pipeline stage is a fetch stage in the first pipeline and the partner pipeline stage is a decode stage in the second pipeline, that decode stage being configured to decode the coprocessor instruction upon receipt of the token (Gearty, Fig. 4: the fetch stage of the first pipeline and the decode stage of the second are connected and the second pipeline can decode instructions that are sent by the first pipeline).

13. As per claim 5, Gearty and Martin teach all the limitations of claim 4 as discussed above, where Gearty further teaches the data processing apparatus comprising wherein the fetch stage in the first pipeline is configured to cause a token to be placed in the instruction queue for each instruction in the sequence of instructions (Gearty, col. 11, ll. 1-18: a "go-token" is taught which is use to synchronize the pipeline), and the decode stage in the second pipeline is arranged to decode each instruction upon receipt of the associated token in order to determine whether that instruction is a coprocessor instruction that requires further processing by the coprocessor (Gearty, Fig. 4: the fetch stage of the first pipeline and the decode stage of the second are connected and the second pipeline can decode the instruction that are sent by the first pipeline).

14. As per claim 6, Gearty and Martin teach all the limitations of claim 1 as discussed above, where Gearty further teaches the data processing apparatus comprising wherein one of the at least one synchronizing queues is a cancel queue (Gearty, col. 7-8: the

table shows the ifu_fpu_cancel_wb queue which is used to cancel instructions), the predetermined pipeline stage is in the first pipeline and is arranged to cause to be placed in the cancel queue a token identifying whether a coprocessor instruction at that predetermined pipeline stage is to be cancelled (Gearty, col. 7-8: the table shows the ifu_fpu_cancel_wb queue associates itself with an instruction), and the partner pipeline stage is in the second pipeline and is configured upon receipt of the token from the cancel queue, and if the token identifies that the coprocessor instruction is to be cancelled, to cause that coprocessor instruction to be cancelled (Gearty, col. 7-8: a cancellation will be done on the associated instruction with the ifu_fpu_cancel_wb queue).

15. As per claim 7, Gearty and Martin teach all the limitations of claim 6 as discussed above, where Gearty further teaches the data processing apparatus comprising wherein the predetermined pipeline stage is an issue stage in the first pipeline, and the partner pipeline stage is a stage following an issue stage in the second pipeline (Gearty, Fig. 3; the issue stage is associated with the fetch stage and from the figure, a natural association/connection is present with the fetch stages of both pipelines).

16. As per claim 8, Gearty and Martin teach all the limitations of claim 6 as discussed above, where Gearty further teaches the data processing apparatus comprising wherein the partner pipeline stage is configured upon receipt of the token from the cancel queue (Gearty, col. 7-8: the table shows the ifu_fpu_cancel_wb queue which is used to cancel

instructions), and if the token identifies that the coprocessor instruction is to be cancelled, to remove the coprocessor instruction from the second pipeline (Gearty, col. 7-8: a cancellation will be done on the associated instruction with the ifu_fpu_cancel_wb queue).

17. As per claim 9, Gearty and Martin teach all the limitations of claim 1 as discussed above, where Gearty further teaches the data processing apparatus comprising wherein one of the at least one synchronizing queues is a finish queue (Gearty, col. 7-8: the table shows the ifu_fpu_data_wb queue which is used to complete instructions), the predetermined pipeline stage is in the first pipeline and is arranged to cause to be placed in the finish queue a token identifying permission for a coprocessor instruction at that predetermined pipeline stage to be retired from the second pipeline (Gearty, col. 7-8: the ifu_fpu_data_wb queue associates itself with the instructions to be completed), and the partner pipeline stage is in the second pipeline and is configured upon receipt of the token from the finish queue, and if the token identifies that the coprocessor instruction is permitted to be retired, to cause that coprocessor instruction to be retired (Gearty, col. 7-8: the instructions in the ifu_fpu_data_wb queue will be completed).

18. As per claim 10, Gearty and Martin teach all the limitations of claim 9 as discussed above, where Gearty further teaches the data processing apparatus comprising wherein the predetermined pipeline stage is a write back stage in the first

pipeline, and the partner pipeline stage is a write back stage in the second pipeline (Gearty, col. 7-8: the ifu_fpu_data_wb queue associates the two write back stages).

19. As per claim 11, Gearty and Martin teach all the limitations of claim 1 as discussed above, where Gearty further teaches the data processing apparatus comprising wherein one of the at least one synchronizing queues is a length queue, the predetermined pipeline stage is in the second pipeline and is arranged, for a vectored coprocessor instruction, to cause to be placed in the length queue a token identifying length information for the vectored coprocessor instruction, and the partner pipeline stage is in the first pipeline and is operable upon receipt of the token from the length queue to factor the length information into the further processing of the vectored coprocessor instruction within the first pipeline (Gearty, col. 5, ll. 54-59: module 124 can be used for vector processing).

20. As per claim 12, Gearty and Martin teach all the limitations of claim 11 as discussed above, where Gearty further teaches the data processing apparatus comprising wherein the predetermined pipeline stage is a decode stage in the second pipeline, and the partner pipeline stage is a first execute stage in the first pipeline (Gearty, Fig. 4: a connection exists between the decode stage in the second pipeline, and the executing stage in the first pipeline).

21. As per claim 13, Gearty and Martin teach all the limitations of claim 1 as discussed above, where Gearty further teaches the data processing apparatus comprising wherein one of the at least one synchronizing queues is an accept queue, the predetermined pipeline stage is in the second pipeline and is arranged to cause to be placed in the accept queue a token identifying whether a coprocessor instruction in that predetermined pipeline stage is to be accepted for execution by the coprocessor, and the partner pipeline stage is in the first pipeline and is configured upon receipt of the token from the accept queue, and if the token identifies that the coprocessor instruction is not to be accepted, to cause that coprocessor instruction to be rejected by the main processor (Gearty, col. 10, ll. 14-20: an accept signal is taught and no further instructions are issued until an accept signal is received).

22. As per claim 14, Gearty and Martin teach all the limitations of claim 13 as discussed above, where Gearty further teaches the data processing apparatus comprising wherein the predetermined pipeline stage is an issue stage in the second pipeline, and the partner pipeline stage is a second execute stage in the first pipeline (Gearty, col. 10, ll. 14-20: an accept signal is taught and no further instruction are issued until an accept signal is received).

23. As per claim 15, Gearty and Martin teach all the limitations of claim 14 as discussed above, where Gearty further teaches the data processing apparatus comprising wherein the partner pipeline stage is configured upon receipt of the token

from the accept queue, and if the token identifies that the coprocessor instruction is not to be accepted, to remove the coprocessor instruction from the first pipeline (Gearty, col. 10, ll. 14-20: an accept signal is taught and no further instruction are issued until an accept signal is received).

24. As per claim 16, Gearty and Martin teach all the limitations of claim 1 as discussed above, where Gearty further teaches the data processing apparatus comprising wherein one of the at least one synchronizing queues is a store queue used when the coprocessor instruction is a store instruction configured to cause data items to be transferred from the coprocessor to memory accessible by the main processor, the predetermined pipeline stage is in the second pipeline and is arranged, when processing one of said store instructions, to cause to be placed in the store queue a token identifying each data item to be transferred, and the partner pipeline stage is in the first pipeline and is configured upon receipt of each token from the store queue, to cause the corresponding data item to be transferred to the memory (Gearty, col. 12, ll. 37-67; a store is done utilizing a token and synchronization of the two pipelines).

25. As per claim 17, Gearty and Martin teach all the limitations of claim 16 as discussed above, where Gearty further teaches the data processing apparatus comprising wherein the predetermined pipeline stage is an issue stage in the second pipeline, and the partner pipeline stage is an address generation stage in the first pipeline (Gearty, Fig. 3: the issue stage and address generation is associated with the

fetch stage and from the figure, a natural association/connection is present with the fetch stage of both pipelines).

26. As per claim 18, Gearty and Martin teach all the limitations of claim 1 as discussed above, where Gearty further teaches the data processing apparatus comprising wherein one of the at least one synchronizing queues is a load queue used when the coprocessor instruction is a load instruction configured to cause data items to be transferred from memory accessible by the main processor to the coprocessor, the predetermined pipeline stage is in the first pipeline and is arranged, when processing one of said load instructions, to cause to be placed in the load queue a token identifying each data item to be transferred, and the partner pipeline stage is in the second pipeline and is configured upon receipt of each token from the load queue, to cause the corresponding data item to be transferred to the coprocessor (Gearty, col. 12, ll. 37-67: a load is done utilizing a token and synchronization of the two pipelines).

27. As per claim 19, Gearty and Martin teach all the limitations of claim 17 as discussed above, where Gearty further teaches the data processing apparatus comprising wherein the predetermined pipeline stage is a write back stage in the first pipeline, and the partner pipeline stage is a write back stage in the second pipeline (Gearty, col. 7-8: the ifu_fpu_data_wb queue associates the two write back stages).

28. As per claim 20, Gearty and Martin teach all the limitations of claim 18 as discussed above, where Gearty further teaches the data processing apparatus comprising wherein one of the at least one synchronizing queues is a store queue used when the coprocessor instruction is a store instruction configured to cause data items to be transferred from the coprocessor to memory accessible by the main processor, the predetermined pipeline stage is in the second pipeline and is arranged, when processing one of said store instructions, to cause to be placed in the store queue a token identifying each data item to be transferred, and the partner pipeline stage is in the first pipeline and is configured upon receipt of each token from the store queue, to cause the corresponding data item to be transferred to the memory, and wherein the load instruction and store instruction may be vectored coprocessor instructions defining multiple data items to be transferred, and the apparatus further comprises flow control logic, associated with at least one of the load queue and the store queue, configured to send a control signal to the predetermined pipeline stage to stop issuance of tokens by the predetermined pipeline stage whilst it is determined that the associated load or store queue may become full (Gearty, col. 12, ll. 37-67; a store is done utilizing a token and synchronization of the two pipelines).

29. As per claim 21, Gearty and Martin teach all the limitations of claim 20 as discussed above, where Gearty further teaches the data processing apparatus comprising wherein the flow control logic is provided for the store queue, the flow control logic being operable to issue the control signal upon receiving an indication from

the main processor that the partner pipeline stage cannot accept a data item (Gearty, col. 12, ll. 37-67: a token is used to indicate status).

30. As per claim 22, Gearty and Martin teach all the limitations of claim 21 as discussed above, where Gearty further teaches the data processing apparatus comprising wherein the load queue is a double buffer (Gearty, Fig. 5 and col. 10, ll. 11-13: the load queue recirculates).

31. As per claim 24, Gearty and Martin teach all the limitations of claim 1 as discussed above, where Gearty further teaches the data processing apparatus comprising wherein the main processor is configured, when it is necessary to flush coprocessor instructions from both the first and the second pipeline, to broadcast a flush signal to the coprocessor identifying the tag relating to the oldest instruction that needs to be flushed, the coprocessor being configured to identify that oldest instruction from the tag and to flush from the second pipeline that oldest instruction and any later instructions within the coprocessor (Gearty, col. 7, ll. 6-48; the state can be cleared or flushed).

32. As per claim 25, Gearty and Martin teach all the limitations of claim 24 as discussed above, where Gearty further teaches the data processing apparatus comprising wherein one or more of said at least one synchronizing queues are flushed

in response to said flush signal, with the tag being used to identify which tokens within the queue are to be flushed (Gearty, col. 7, ll. 6-48: the state can be cleared or flushed).

33. As per claim 27, Gearty and Martin teach all the limitations of claim 1 as discussed above, where Gearty further teaches the data processing apparatus comprising wherein a plurality of said coprocessors are provided, with each synchronizing queue coupling a pipeline stage in the main processor with a pipeline stage in one of the coprocessors (Gearty, col. 1, ll. 14-28: as the chip may have multiple modules, wherein modules can be FPUs).

34. As per claim 28, Gearty and Martin teach all the limitations of claim 1 as discussed above, where Gearty further teaches the data processing apparatus comprising wherein the data processing apparatus has a synchronous design, such that the tokens are caused to be placed in the queue by the predetermined pipeline stage and are caused to be received from the queue by the partner pipeline stage upon changing edges of a clock cycle (Gearty, col. 9, ll. 39-47: the system is run generally in a synchronous fashion and is out of sync in only rare circumstances).

35. As per claim 29, claim 29 is rejected for reasons similar to that of claim 1; claim 29 is the method claim for the apparatus claim of claim 1.

36. As per claim 30, claim 30 is rejected for reasons similar to that of claims 2, 4, 7, 10, 12, 14, 17 and 19; claim 30 is the method claim for the apparatus of claims 2, 4, 7, 10, 12, 14, 17 and 19.

37. As per claims 31-39, 41-42 and 44-45, claims 31-39, 41-42 and 44-45 are rejected for reasons similar to that of claims 3, 6, 9, 11, 13, 16, 18, 20, 21, 24-25 and 27-28.

VII. CLOSING COMMENTS

Conclusion

a. STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. 707.07(i)**:

a(1) CLAIMS REJECTED IN THE APPLICATION

Per the instant office action, applicant's amendment necessitated the new ground(s) of rejection presented in this Office action; claims 1-22, 24-25, 27-39, 41-42 and 44-45 have received a final action on the merits. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

b. DIRECTION OF FUTURE CORRESPONDENCES

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun-Kuan (Mike) Lee whose telephone number is (571) 272-0671. The examiner can normally be reached on 8AM to 5PM.

IMPORTANT NOTE

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alford Kindred can be reached on (571) 272-4037. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

November 13, 2007

Chun-Kuan (Mike) Lee
Examiner
Art Unit 2181

ALFORD KINDRED
SUPERVISORY PATENT EXAMINER